# Zeen Fang

B.Eng. Candidate, Microelectronics Science and Engineering
Central South University
Mobile: +86-17770387931
Email: 8203231006@csu.edu.cn

## EDUCATION

**Central South University** 09/2023–06/2027
*B.Eng. in Microelectronics Science and Engineering* GPA: 89.43/100

**High-score modules:** Advanced Mathematics A I/II (97/97), Probability and Statistics (97), Linear Algebra (95), University Physics C II (98), Course Design of EDA Technology and Application (94), Scientific Computing and MATLAB Language (92), Signals and Systems (93), Large-Scale Integrated Circuit Design (94), and Heat Transfer Theory (91).

**Core major modules:** Semiconductor Device Physics, Circuit Theory, Analog/Digital Electronic Technology, EDA Technology and Application, Microelectronics Manufacturing Engineering, Microelectronics Packaging Engineering, and Manufacturing and Testing of Semiconductor Integrated Devices.

## RESEARCH INTERESTS

Power management ICs, DC-DC converters, LDOs, analog IC design, semiconductor device simulation, and device-circuit co-design.

## RESEARCH AND PROJECT EXPERIENCE

**Competition Team Project** 07/2026
*LDO Design and Validation: Zengyi Huichuang Track*

- **IC design and physical verification:** Contributed to a 1.8 V LDO in SMIC 180 nm CMOS, including PMOS/BGR/OTA/feedback-compensation design, simulation, layout, Calibre DRC/LVS/PEX, and post-layout verification.
- **Results and regional final:** For 3.0–5.0 V input and 0.1–200 mA load, post-layout results reached $V_{\text{drop}} \approx 126$ mV, $I_q = 8.745$–$9.173$ $\mu$A, 65.91–69.27 dB PSRR at 1 kHz, and 67.92°–74.54° PM; characterized TIP42C/BD139 devices with IECUBE-3835 and built/tested a 25 V-to-12 V semi-discrete LDO.

**Independent Research Project** 03/2025–Present
*Memristor-Based Read-Write Interface Design for Neural Networks*

- **Interface and evaluation:** Proposed a two-phase read-write separation interface using mutually exclusive PMOS/NMOS switching; evaluated cycle consistency, noise, frequency response, dynamic switching, and parasitic effects.
- **Research output:** First-author paper published in *Electronics*, 15, 2333 (2026).

**Independent Research Project** 07/2025–04/2026
*Short-Channel Effects and RF Performance in Top-Gate $In_2O_3$ Thin-Film Transistors*

- **Simulation and modeling:** Performed 2-D device simulations of scaled top-gate $In_2O_3$ FETs with a 1.5 nm channel to investigate short-channel effects.
- **Data analysis and output:** Extracted DC/RF parameters across gate lengths and identified a critical transition near 100 nm; third-author paper published in *Micromachines*, 17, 567 (2026).

## PUBLICATIONS

- **Fang, Z.**, Zhu, M., Xu, H., & Zhang, L. (2026). Memristor-Based Read-Write Interface Design for Neural Networks: A Comparative Study of Linear-Drift and VTEAM Models. *Electronics*, 15, 2333.
- Xu, H., Zhu, M., Fang, Z., & Zhang, L. (2026). Numerical Investigation of Short-Channel Effects and RF Performance in Top-Gate $In_2O_3$ Thin-Film Transistors. *Micromachines*, 17, 567.
- **Fang, Z.** (2026). Construction of a Second-Order Memristor SPICE Circuit Model and Neuromorphic Characteristics Analysis. Manuscript in preparation; target journal: *IEEE TCAS-I*.

## AWARDS AND HONOURS

Second Prize, National Final; First Prize, Central China Regional Final — 10th National College Student IC Innovation and Entrepreneurship Competition (Zengyi Huichuang Track) 2026
Second Prize, National Preliminary Round (Humanoid Sprint), 28th China Robot and Artificial Intelligence Competition 2026
First Prize, Hunan Division, 16th Chinese Mathematics Competition for College Students (Non-Mathematics Category A) 2024
First Prize, 8th Hunan Provincial College Students Mathematics Competition (Non-Mathematics Category A) 2024
Highpower International Scholarship — Excellent Student Award 2024
Outstanding Student, Central South University 2023–2024
Second-Class Academic-Year Scholarship, Central South University 2024

## SKILLS AND ACTIVITIES

- **Technical tools and methods:** PSpice, Cadence Allegro, MATLAB, LabVIEW, LaTeX, semiconductor device simulation, and circuit modeling.
- **English proficiency:** CET-6: 576.